



VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN  
 [AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]  
 Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

**Question Paper Code: 70062**

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – FEB. 2025

First Semester

VLSI Design

P23VD102 – VLSI DIGITAL SIGNAL PROCESSING

(Regulation 2023)

Time: Three Hours

Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels	K1 – Remembering	K3 – Applying	K5 - Evaluating
(KL)	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Find the loop bound of the data flow graph shown in Fig.1.	2	K1	CO1

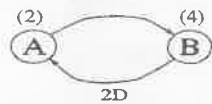


Fig.1

2.	Draw the two level pipelined and parallel processing structure for the data path shown in Fig.2.	2	K1	CO1
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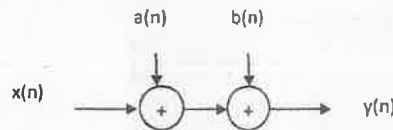


Fig.2.

3.	Show that retiming does not change the number of delays in any cycle.	2	K2	CO2
4.	Define algorithmic strength reduction in filter.	2	K1	CO2
5.	Define Lagrange interpolation theorem.	2	K1	CO3
6.	Sketch the pole-zero plot of first order original and pipelined IIR filter. Assume M=8.	2	K2	CO3
7.	Show that the transfer function of a filter doesn't change when a scaling operation is applied to it.	2	K2	CO4
8.	Find the canonical signed digit (CSD) representation of the given number: 0.00111100.	2	K2	CO4
9.	Define clock skew.	2	K1	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.	Questions	Marks	KL	CO
11. a)	Calculate the iteration bound of the given Fig.3 using longest path matrix algorithm.	13	K2	CO1

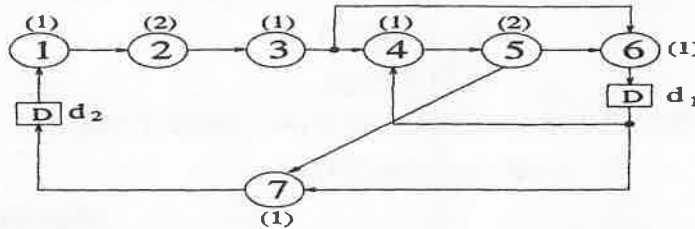


Fig.3

(OR)

b)	Consider a 3-tap filter described by the equation $y(n)=ax(n)+bx(n-1)+cx(n-2)$ . Compute a parallel processing structure. Also, discuss how parallel processing reduces the power consumption of a system.	13 (6+7)	K2	CO1
12. a)	Describe the application of the unfolding technique for sample period reduction and parallel processing using data flow graphs.	13 (6+7)	K2	CO2
(OR)				
b)	Explain a parallel FIR structure using the algorithmic strength reduction technique.	13	K2	CO2
13. a)	Construct a 2*2 convolution algorithm using the Cook – Toom algorithm with $\beta = 0, +1, -1$ .	13	K3	CO3
(OR)				
b)	Explain the look-ahead pipelining and clustered look-ahead pipelining for the given first order IIR filter $H(z) = \frac{1}{1-0.5z^{-1}}$ .	13	K2	CO3
14. a)	Explain the computation of scaling and round-off noise in both unscaled and scaled second order filters.	13	K2	CO4
(OR)				
b)	Consider two 4-bit numbers $A=a_3a_2a_1a_0$ and $B=b_3b_2b_1b_0$ . Construct a parallel carry ripple array multiplier to multiply A and B.	13	K3	CO4
15. a)	Explain the synchronous pipelining and clock styles in detail.	13	K2	CO5

(OR)

- b) Describe the wave pipelining. Compare wave pipelining with asynchronous pipelining. 13 K2 CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.	Questions	Marks	KL	CO
16. a)	This problem considers design of a fast 6-point IDCT structure based on decimation-in-frequency approach.		K3	CO2
	i. First obtain a 3-point IDCT butterfly for computing	8		
	$x(n) = \sum_{k=0}^2 X(k) \cos \frac{(2n+1)k\pi}{6}; n = 0,1,2.$			
	ii. Using the 3-point IDCT butterfly in (i) implement the 6-point fast IDCT decimation-in-frequency structure. Calculate the total number of multiplication and add operations in this structure.	7		

(OR)

- b) Compute the 4-unfolded DFG of the original DFG shown in Fig.4 and the 3-unfolded DFG of the original DFG shown in Fig.5. 8+7 K3 CO2



Fig.4

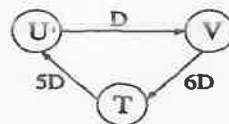


Fig.5